Dynamically Growing Neural Network Architecture for Lifelong Deep Learning on the Edge

Duvindu Piyasena*, Miyuru Thathsara†, Sathursan Kanagarajah‡, Siew-Kei Lam§ and Meiqing Wu¶

*†§¶Nanyang Technological University, Singapore
{*gpiyasena, †assklam, ¶meiqingwu}@ntu.edu.sg, ‡mthathsara@outlook.com, †ksathursan1408@gmail.com

Abstract—Conventional deep learning models are trained once and deployed. However, models deployed in agents operating in dynamic environments need to constantly acquire new knowledge, while preventing catastrophic forgetting of previous knowledge. This ability is commonly referred to as lifelong learning. In this paper, we address the performance and resource challenges for realizing lifelong learning on edge devices. We propose a FPGA based architecture for a Self-Organization Neural Network (SONN), that in combination with a Convolutional Neural Network (CNN) can perform class-incremental lifelong learning for object classification. The proposed SONN architecture is capable of performing unsupervised learning on input features from the CNN by dynamically growing neurons and connections. In order to meet the tight constraints of edge computing, we introduce efficient scheduling methods to maximize resource reuse and parallelism, as well as approximate computing strategies. Experiments based on the Core50 dataset for continuous object recognition from video sequences demonstrated that the proposed FPGA architecture significantly outperforms CPU and GPU based implementations.

Keywords—Deep learning, lifelong learning, continual learning, incremental learning, self-organization, FPGA

I. INTRODUCTION

Recent advancements in deep learning and computing technology have enabled deep learning models to be deployed in a wide range of embedded applications for self-driving cars, autonomous robots, etc [1], [2]. Such applications typically encounter settings that are not available during training. Ideally, the models should be able to acquire new knowledge in real-time, while not interfering with previous knowledge. This ability is referred to as lifelong learning which is now an active area of research [3]. The following are desired for lifelong learning in embedded applications.

Real-time learning. In conventional deep neural networks (DNNs), learning is performed on large data over many hours or days. However, a lifelong learning model needs to learn quickly from a few samples in real-time.

Learning at the edge. Deep learning models are usually trained using GPUs in the cloud, which has several limitations, e.g., 1) network connectivity cannot always be guaranteed, 2) privacy concerns of sending data to cloud. Performing learning on the edge device overcomes these problems.

Custom computing. Embedded systems have tight computational and memory constraints, and they often run on strict power budgets. Lifelong algorithms deployed on the edge will need design strategies that take full advantage of the compute capabilities of the target platform.

Meeting the above requirements is challenging. Firstly, it has been shown that when connectionist neural networks are trained incrementally with new knowledge, the models undergo catastrophic forgetting of previous knowledge [4]. This can be solved naively by storing all the past data and shuffling them with new data when training on new tasks. However, it is not practical to store such large datasets due to memory resource constraints and privacy concerns. Secondly, back-propagation based learning that is used in state-of-the-art deep learning models require cloud grade GPU or specialized accelerators like TPU [5], due to high compute and memory requirements. Despite this, training a model from scratch still takes a long time ranging from hours to a few days. In addition, these cloud grade computing platforms are ill-suited for deployment in edge devices due to their high energy consumption. These challenges can only be overcome with new deep learning models capable of unsupervised lifelong learning and custom hardware implementations of the same.

In this paper, we propose an FPGA based custom hardware architecture for class-incremental lifelong learning, targeting object classification task in edge devices. The proposed model is based on a Self-Organization Neural Network (SONN), called Grow When Required (GwR) artificial neural network [6]. GwR network leverages on local learning and self-organization with dynamic neuron/connection formation/pruning. We combined a backbone CNN network as a feature extractor with the GwR based SONN as a classifier to achieve lifelong learning, and propose a novel FPGA architecture for the SONN. Our main contributions are:

- Novel hardware design of SONN that performs class-incremental learning for object classification. This is the first work to propose a FPGA architecture for dynamically growing SONN, where the neurons and connections evolve over time. Previously reported hardware implementations of SONN have fixed neurons and connections.
- Efficient scheduling methods to maximize resource reuse and parallelism. Bit-width quantization and approximate computing are used to reduce hardware complexity.
- Proposed FPGA architecture significantly outperforms CPU and GPU implementations on the Core50 dataset for continuous object recognition from video streams.

1The terms continual learning, incremental learning are also used commonly in literature.
II. RELATED WORK

A. Lifelong Learning

Lifelong learning refers to learning new tasks efficiently, while not catastrophically forgetting previous tasks. The current approaches fall under three categories: 1) Regularization 2) Architectural 3) Memory Rehearsal [3], [7]. Regularization approaches penalize changes to parameters important to previous knowledge by modifying the regular loss [8], [9], [10]. Architectural approaches dynamically change the model architecture over time to accommodate new knowledge [11], [12]. In memory rehearsal methods, subset of training data are buffered and replayed when learning new tasks [13], [14].

B. Self-Organization and Lifelong Learning

Our work adopts an architectural approach to address catastrophic forgetting with a SONN. SONN is a family of artificial neural networks, which is used for topology learning of a feature space through an unsupervised learning method named competitive learning [6], [15], [16]. Various types of SONNs have been proposed in literature, with the most popular one being the Self-Organized Map (SOM) [15]. However, the fixed network size and time-decaying learning rule limit its ability to learn continuously. The work in [16] proposed to periodically grow a network of neurons. GwR [6] extends [16] by replacing the periodic neuron adding criteria with a rule that adds neurons based on network activity. Recently, SONNs have been used in combination with CNNs to perform lifelong learning for object classification [12], [17]–[19]. Particularly inspired by [12], we combine a CNN with a SONN based on GwR to demonstrate the feasibility of performing lifelong learning under edge constraints using custom hardware acceleration.

C. FPGA based lifelong learning

The works in [20], [21] propose to accelerate conventional DNN training using multi-FPGA platforms. Recent works [22]–[24] propose FPGA based lightweight models particularly for lifelong learning. The work in [22] relies on a Hebbian learning rule, while [23], [24] rely on a product quantization strategy for lifelong learning. Similar to the proposed work, these methods leverage on local learning and learns quickly from few samples. However, contrary to our work, they rely on a fixed set of neurons, which limits the ability to autonomously learn from non-stationary data distributions.

III. PROPOSED LIFELONG LEARNING MODEL

The proposed model, shown in Fig. 1, combines a Convolutional Neural Network (CNN) and a SONN, where the latent features extracted from the CNN are fed into the SONN that acts as the classifier. As the model is exposed to new classes, the SONN evolves while CNN layers remain static.

CNN models trained on large datasets (e.g., Imagenet [25]) have been shown to perform well, as generic feature extractors [26]. We have used the Resnet-18 CNN model, pre-trained on Imagenet. The latent features are extracted from the last convolutional layer (Avg Pool) of Resnet-18 of dimension $(D_f)$ 512, and the subsequent Fully-Connected layer is discarded.

The SONN is based on the GwR network [6]. In this paper, we will only discuss the hardware architecture of the classifier (i.e. SONN), since there are already many works on hardware implementation of CNNs [27]–[30].

A. SONN Algorithm

The SONN performs unsupervised learning on input features and creates a discrete topology representation of the feature space using a dynamically growing set of neurons $(N)$ and connections $(C)$. During training, neurons are added progressively to better represent input topology, while connections are formed between similar neurons following the Hebbian learning principle [31].

Each neuron $(i \in N)$ has several parameters: a) weights vector $(w_i)$, which determines neuron position in the feature space, b) habitation counter $(H_i)$, measure of how frequent the neuron has fired, c) class probability vector $(p_i)$, probability of association to all the classes, and d) connectivity graph $(G(V_i,E_i))$, graph of connected neurons $(V_i)$ and connections $(E_i)$. Each connection $(c \in C)$ has an associated age $(age_c)$.

Algorithm 1 Proposed SONN pseudo-code

```
1: [Step 1 : Winner Selection Phase (WSEL)]
2: for $i = 1$ to $N_{curr}$ do // inter-neuron loop
3:   for $j = 1$ to $D_f$ do // intra-neuron loop
4:       $dist_i \leftarrow dist_i + |x_j-w_{i,j}|$
5:   end for
6:   if $dist_i < dist_{b_i}$ then
7:     $\{b_1,dist_{b_1}\},\{b_2,dist_{b_2}\} \leftarrow \{i,dist_i\}, \{b_i,dist_{b_i}\}$
8:   else if $dist_i < dist_{b_i}$ then
9:     $\{b_1,dist_{b_1}\},\{b_2,dist_{b_2}\} \leftarrow \{b_1,dist_{b_1}\}, \{i,dist_i\}$
10: end if
11: end for
12: if $(dist_{b_i} > dist_T$ and $H[dist_i] < b_i)$ then
13:   [Step 2 : Neuron Addition Phase (NADD)]
14:   for $j = 1$ to $D_f$ do // intra-neuron loop
15:     $w_n \leftarrow (x_j+w_{b_1,j})/2$
16:   end for
17:   $h_n \leftarrow 0$, $p_{n,l} \leftarrow 1$, and $p_{n,j} \leftarrow 0, j \neq l$
18:   Connect $n$ with $b_1, b_2$ and disconnect $b_1, b_2$
19: else
20:   [Step 3 : Neuron Train Phase (NTRAIN)]
21:   for $i = 1$ to len(neigh) do // inter-neuron loop
22:     for $j = 1$ to $D_f$ do // intra-neuron loop
23:       $w_{i,j} \leftarrow w_{i,j} + \epsilon \cdot H[dist_i] \cdot (x_j-w_{i,j})$
24:     end for
25:     $h_i \leftarrow h_i + 1$, $p_{n,l} \leftarrow p_{n,l} + 1$
26:   end for
27: end if
```

Algorithm 1 describes the training of SONN, which consists of three main steps: a) Winner Selection (WSEL), b) Neuron Add (NADD), and Neuron Train (NTRAIN).

1) Step 1. Winner Selection (WSEL): Upon receiving an input feature vector $(x)$, SONN computes the Manhattan distance between input $(x)$ and weights vectors $(w)$ of all neurons and the 2 neurons with the least distance to the input
are selected as best matching units, BMU-1 ($b_1$) and BMU-2 ($b_2$). The class with maximum probability of association ($\arg\max(p_n)$) is predicted as the classification output. During training, if BMU-1 is both distant from input ($\text{dist} > \text{dist}_T$) and sufficiently mature ($H[h_{b1}] < h_T$), a new neuron is added to SONN to better represent the input (Step 2). Consequently, neurons that are sufficiently dissimilar to the input and well habituated are not modified, preventing catastrophic interference to consolidated knowledge of the network. On the other hand, if this condition is not met, BMU-1 and its connected neighbour neurons ($\text{neigh}_{b1} = b_1 \cup V_{b1}$) are trained.

2) Step 2. Neuron Add (NADD): If a neuron is added, it ($n$) is assigned weights ($w_n$) associated with BMU-1 ($w_{b1}$) and input feature vector ($x$). The class probability vector of the neuron ($p_n$) is initialized to associate with the class of the training sample ($l$). The new neuron is connected to both BMU-1 and BMU-2, and if a connection existed between BMU-1 and BMU-2, it is removed. The changes to the connectivity graphs ($G(V, E)$) of the three neurons are shown in Eq. 1.

$$
\begin{align*}
V_{b1} & = V_{b1} \cup \{n\}/\{b_2\}, V_{b2} = V_{b2} \cup \{n\}/\{b_1\}, \\
E_{b1} & = E_{b1} \cup \{(n, b1)\}/\{(b_1, b2)\}, \\
E_{b2} & = E_{b2} \cup \{(n, b2)\}/\{(b_1, b2)\}, \\
V_n & = \{b_1, b2\}, E_n = \{(n, b1), (n, b2)\}
\end{align*}
$$

(1)

3) Step 3. Neuron Train (NTRAIN): If a neuron is not added, then the weights of BMU-1 and its connected neighbours ($\{w_i| i \in \text{neigh}_{b1}\}$) are modified such that they are closer to the input in the feature space, and their habituation counters are updated to decrease response of neurons to further training. Next, the age of all connections of BMU-1 ($E_{b1}$) are increased by a step, except the one between BMU-1 and BMU-2 ($b_1, b_2$). If the latter is present, $\text{age}_{(b_1, b_2)}$ is reset to zero. Otherwise, a new connection is created with age set to zero. Finally, the class probability vector of BMU-1 ($p_{b1}$) is updated to increase its association to class label of training input.

As the SONN is adapted only at the local neighbourhood that is most similar to the input ($\text{neigh}_{b1}$), catastrophic interference to parameters unrelated to the current input is prevented. This local adaptation is lightweight in terms of computation and memory requirements, compared to back-propagation based learning with entire model adaptation. The dynamically growing nature of the SONN enables the model to adapt to non-stationary data streams and grow accordingly. Most importantly, the proposed SONN has inherent parallelism of vector computations which lends itself well towards custom hardware implementations.

IV. PROPOSED HARDWARE ARCHITECTURE

A. Overview of Architecture

Fig. 2 shows the proposed architecture, which consists of four main blocks: PE Matrix, Neuromodulator, Associative Memory and Controller. PE Matrix performs vector computations of neuron weights: distance calculation of input to weights of all neurons and winner selection during WSEL, calculation of new neuron weights during NADD, and updating weights during NTRAIN. Neuromodulator schedules the operations on the PE matrix during training (NTRAIN and NADD), while maintaining neighbourhood graphs of all neurons and state of connections. Associative memory maintains the probability scores of each class per each neuron. These three blocks are controlled and synchronized by the Controller.

B. Hardware Approximations

The following approximations were applied to various operations of the GwR algorithm.

Quantization. Inputs and parameters (originally in floating-point) were quantized to 8-bit integers [32]. In NTRAIN, the learning rate was rounded to nearest power-of-2 values to replace costly multiplications with bit-shift operations.

Distance Computation. The Euclidean distance ($d_i = ||x - w_i||$) in GwR is replaced with the relatively lighter Manhattan distance, $d_i = ||x - w_i||_1$.

Activity Calculation. In GwR, the activity of BMU-1 ($\text{act} = \exp(-d_{b1})$) is thresholded ($\text{act} < \text{act}_T$) to decide on the addition of a new neuron. To avoid the exponential calculation, this was replaced with distance thresholding ($\text{dist}_{b1} > \text{dist}_T$).

Habituation Counter. Each time a neuron is trained during NTRAIN, its habituation counter is updated by $\tau \cdot 1.05 \cdot (1 - H[h_{b1}]) - \tau$, ($\tau$ is a constant). To reduce the number of expensive arithmetic operations at runtime, we precomputed
100 discrete values offline. These values were quantized to 8-bit and stored in a ROM ($H$). A pointer ($h$) is maintained per neuron to point to its current value in $H$, which is incremented each time the neuron is trained (Algorithm 1, line 25).

C. Exploiting Parallelism

Parallelism is exploited for the vector processing operations involving neuron weights ($w$) in WSEL, NADD and NTRAIN. These operations have 2 kinds of parallelism: inter-neuron and intra-neuron parallelism, which refer to concurrent operations between neurons and within a neuron respectively. Both parallelisms are achieved in the proposed hardware architecture by unrolling inter-neuron loops (Algorithm 1, lines 2, 21) and intra-neuron loops (lines 3, 14, 22) by $N_c$ and $N_r$ factors respectively. The unrolled design is executed in a systolic array of processing elements (PE Matrix). Each PE is connected with adjacent PEs supporting pipelined dataflow as shown in Fig. 3. This allows pipeline execution of both inter-neuron and intra-neuron loops, which results in further parallelism.

D. Functional Units

1) PE Matrix: PE matrix consists of a set of Processing Columns (PC), which operates under three different configurations: a) Pipelined array (WSEL), b) Semi-broadcast array (NADD), and c) full broadcast array (NTRAIN). Each configuration supports different dataflow requirements in the three steps while maximizing parallelism, as shown in Fig. 3. Each SONN neuron is organized as a Processing Column (PC). A PC contains an array of processing elements (PE), multipliers to perform computations, and a memory bank for storing weights ($w$) and habituation pointers ($h$) of its local neurons, as shown in Fig. 4a. When neurons are progressively added to SONN, they are assigned a PC in a modulo round-robin manner. Thus, when the $m^{th}$ neuron is added, $m \mod N_{th}$ PC will store its weights ($w_m$) and habituation pointers ($h_m$), and all its computations as per Algorithm 1 will be performed locally. Due to round robin assignment, the neurons are evenly distributed across the PCs, with each PC supporting up to $\lceil N_{max}/N_c \rceil$ neurons. The inter-neuron loops are unrolled and executed in parallel by the PCs, while intra-neuron loops are unrolled and executed in parallel within each PC.

During WSEL, each PC computes distance between input ($x$) and neuron weights ($w$) that are local to the column. Each PE computes distance between an input and a weight vector element followed by an accumulation of distance from its upstream neighbor. This operation of the $j^{th}$ PE of $i^{th}$ PC is described in line 4 of Algorithm 1.

As shown in Fig. 3a, in each PC, the partial accumulated distance values are sent downstream (blue arrows). To synchronize with upstream partial accumulated inputs, $vbuff$ delays input to each PE row in the PC. The final accumulated distance is sent to a local comparator unit (Comp), where it gets compared with the two current BMU-1 and BMU-2 distances ($\text{dist}_{b_1}, \text{dist}_{b_2}$) received from downstream comparators. BMU-1 and BMU-2 are updated according to Algorithm 1, lines 6-10. The updated BMU-1 and BMU-2 are forwarded to the next comparator (orange arrows). To synchronize with comparator dataflow, input to each PC is delayed by $hbuff$.

During NADD, the PC containing BMU-1 ($PC_{src} = b_1 \mod N_c$) computes the weights of new neuron added ($n$) as described by Algorithm 1, lines 14-16. The computed weights ($w_n$) are transferred from the $PC_{src}$ to $PC_{dest}$, by shifting them horizontally across the PE matrix from one column to another. This is shown in Fig. 3b, where red arrows represent the movement of weights. The weights are eventually stored in $PC_{dest}$, which is determined by the neuromodulator.

In NTRAIN, neurons in the set $\text{neigh}_{b_i}$ are modified according to Algorithm 1, Step 3, by the corresponding PCs belonging to the set $PC_{train} = \{x \mod N_c | \forall x \in \text{neigh}_{b_i}\}$ in parallel, while other PCs are idle. If a PC has multiple neurons to be trained, updates are queued and performed sequentially by that PC. Each PE in a PC performs weights update of a single weight vector element independently of other PEs. The behaviour of $j^{th}$ PE when PC updates the $i^{th}$ neuron weights is shown in Algorithm 1, line 23. The PE computes difference between $x$ and $w$ vector elements ($x_j - w_{i,j}$), and a multiplier bank local to each PC performs $-H[h_i, (x_j - w_{i,j})]$, and the result is added to $w_{i,j}$ inside PE.

Fig. 4c shows the internal structure of a PE, where the different computations required for the three steps are performed using shared arithmetic resources. The operation of the PE is controlled by the controller and neuromodulator, depending on the operational steps and the role of the corresponding PC. Based on the resource constraints, intra-neuron loops of Algorithm 1 are folded by a factor of $D_f/N_r$. Weights and habituation pointers of neurons are stored in BRAM blocks dedicated to each PC, so that the computations are not delayed by external memory accesses. Each PC requires $8 \cdot D_f \cdot \lceil N_{max}/N_c \rceil$ and $8 \cdot (100+\lceil N_{max}/N_c \rceil)$ bits for weights.
Neuromodulator: During NADD and NTRAIN, only a subset of PCs are active at a time. The neuromodulator schedules computations to these required PCs during these two steps. To control individual PCs, the neuromodulator consists of a scheduler block with $N_C$ scheduler units (sch), each connected to a PC as shown in Fig. 2. The neuromodulator also maintains connectivity graphs ($G$) for all SONN neurons in the form of lists of neighbour neurons ($V$) and connections ($E$) of each neuron, in two separate BRAM based memories.

In NADD, $PC_{src}$ computes the new neuron weights ($w_n$) and shift them through PCs to $PC_{dest}$. The individual scheduler units set $PC_{src}$ to compute new neuron weights, $PC_{dest}$ to store the weights, PCs in between these to bypass the weights, and other PCs to idle. Additionally, the connectivity graphs of BMU-1 ($V_{b1}$) and BMU-2 ($V_{b2}$) are updated in the $V$ and $E$ memories, while a new entry ($G(V_n, E_n)$) is created in each of them for the new neuron, as explained in Eq. 1.

In NTRAIN, the neuromodulator schedules PCs in the set $PC_{train}$ to train $neighbor_{b1}$ set of neurons. For this, neighbour neuron list of BMU-1, $V_{b1}$, is read from $V$ memory and the memory bits containing $neighbor_{b1}(b_1 \cup V_{b1})$ set of neurons is scanned by all $N_C$ scheduler units in parallel. After which, each scheduler unit identifies neuron(s) associated with the connected PC. The set of neurons to be trained in the $j^{th}$ PC is denoted as $N_j=[n/m \mod N_c=j, \forall n \in neighbor_{b1}]$. Consequently, $PC_j$ updates $N_j$ neurons iteratively as per Algorithm 1, line 23, while each PC operates independently in parallel.

The design assumes maximum neighbours of any neuron to be $Neigh_{max}$, which is empirically determined. Each neuron and connection is identified by an identifier of $log_2(N_{max})$ and $log_2(C_{max})$ bits respectively. Therefore the on-chip BRAM storage requirement for the two memories, $V$ and $E$ is $8 \cdot N_{max} \cdot Neigh_{max} \cdot (log_2(N_{max}) + C_{max})$.

3) Associative Memory: This unit ($P$) maintains the class probability vectors ($p$) of all neurons on BRAM, which is updated during NADD and NTRAIN phases as per Algorithm 1, lines 17, 25. A single probability is represented by 8 bits. Hence, memory requirement of $P$, is $8 \cdot N_{classes} \cdot N_{max}$ bits.

4) Controller: The controller manages the dataflow of the PE matrix in the three steps by feeding activations into the PE Matrix in a synchronous manner, and synchronizing PE Matrix and neuromodulator operations.

E. Latency and Storage Analysis

As shown in Fig. 5, as neurons are added, the latency of WSEL increases linearly in a piece-wise manner due to the $N_c$ inter-neuron parallelism of PE Matrix. The latencies of NADD and NTRAIN do not increase monotonically with neurons. NADD latency is a function of $PC_{src}$ and $PC_{dest}$, due to the pipelined data movement explained earlier. The latency of NTRAIN is dependant on the maximum neurons to be trained in a single column ($max_{schr}$). The mean and standard deviation of the latency distributions of NADD and NTRAIN are summarised in Table II.

The proposed design assumes an upper-bound of neuron growth and connection formation, with maximum limit of neurons $N_{max}$, neighbours per neuron $Neigh_{max}$, and connections $C_{max}$. The bounds are constrained by the availability of on-chip BRAM, and could be extended by storing neuron parameters in an off-chip memory. The total storage requirement of the design is given by Eq. 2.

$$S_T = 8 \cdot N_{max} \cdot (D_F + 1) + 100 \cdot N_c + N_{classes} \cdot N_{max} + 8 \cdot C_{max} \cdot Neigh_{max} \cdot (log_2(N_{max}) + C_{max})$$

V. EXPERIMENTAL RESULTS

We analyze and evaluate our proposed method on Core50, a popular benchmark dataset developed specifically for continuous object recognition from video sequences [33]. The dataset consists of 50 object classes belonging to 10 categories, with classification performed at both levels. We use the train/test split suggested in [33], but images are sampled at 1fps from the video stream as consecutive images are similar. The model was evaluated under New Classes (NC) scenario, where model was trained sequentially in a class-incremental manner.

The following baselines are used. A vanilla Resnet18 model was trained with stochastic gradient descent (SGD) in a class-incremental manner (Naive) and using entire dataset at once (Cumulative). Original GwR model (GwR) was used to evaluate the proposed approximations. Additionally, the proposed model is compared with two popular lifelong learning methods for class incremental learning (iCaRL [13] and ExStream [34]).

![Fig. 5: WSEL latency. (Freq. = 200Mhz)](image)

(a) Neuron Growth  
(b) Connection Growth

Fig. 6: Model growth comparison
TABLE I: Model performance evaluation

<table>
<thead>
<tr>
<th>Method</th>
<th>Accuracy (%)</th>
<th>Train Time (s)</th>
<th>Mem. requirement (Params + Data, MB)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Object</td>
<td>Category</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Encountered</td>
<td>Encountered</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Classes(Object)</td>
<td>Classes(Object)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>0</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>20</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>40</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>60</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>80</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>100</td>
<td></td>
</tr>
<tr>
<td>Naive</td>
<td>89.64</td>
<td>95.86</td>
<td></td>
</tr>
<tr>
<td>Cumulative</td>
<td>89.64</td>
<td>95.86</td>
<td></td>
</tr>
<tr>
<td>ExStreama</td>
<td>67.45</td>
<td>81.68</td>
<td>70.92/139.75</td>
</tr>
<tr>
<td>f</td>
<td></td>
<td></td>
<td>1.906 ± 1.563</td>
</tr>
<tr>
<td>iCaRLb</td>
<td>36.99</td>
<td>52.33</td>
<td>2359.4/2359.4</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>136 ± 75</td>
</tr>
<tr>
<td>GwRC</td>
<td>62.47</td>
<td>82.3</td>
<td>37.37/85.46</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1.53 ± 0</td>
</tr>
<tr>
<td>Proposedd</td>
<td>64.25</td>
<td>83.45</td>
<td>20.17/66.69</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0.73 ± 0</td>
</tr>
</tbody>
</table>

TABLE II: Latency (μs) comparison for CPU, GPU and FPGA

<table>
<thead>
<tr>
<th>Step</th>
<th>GPUa</th>
<th>CPU1</th>
<th>FPGA2</th>
</tr>
</thead>
<tbody>
<tr>
<td>WSEL (min-max)</td>
<td>570 - 694</td>
<td>204 - 950.5</td>
<td>0.63 - 4.145</td>
</tr>
<tr>
<td>NTRAIN (mean ± std)</td>
<td>1220 ± 224</td>
<td>734 ± 224</td>
<td>0.484 ± 0.157</td>
</tr>
<tr>
<td>NADD (mean ± std)</td>
<td>1600 ± 720</td>
<td>1080 ± 350</td>
<td>0.487 ± 0.144</td>
</tr>
</tbody>
</table>

A. Accuracy evaluation

The approaches are evaluated based on accuracy, training time and memory requirement. The results are summarised in Table I. The train times were measured using models developed on PyTorch framework [35] and executed on GPU, while memory requirement was calculated from trainable parameters, and data storage, required for lifelong learning. It can be observed that Naive undergoes catastrophic forgetting. Among the lifelong learning models, the proposed SONN exhibits higher accuracy than iCaRL and ExStream in category level, while executing faster and consuming lesser memory. Although, the proposed SONN generates more neurons and connections than GwR as shown in Fig. 6, the memory requirement and runtime is lesser, with slight improvement in accuracy. Hence, the proposed model is clearly more amenable to edge implementation with tight computation and memory constraints. Fig. 7 shows the accuracy change of all methods as classes are encountered.

B. Hardware Comparison

The proposed SONN was implemented with Verilog HDL and synthesized using Xilinx Vivado 2019.1 for Zynq UltraScale+ ZCU9EG at 200MHz. CPU and GPU implementations of the SONN was developed using PyTorch framework [35], for benchmarking the proposed hardware.

Table II shows the performance of all devices for the three steps separately per video sample. The range of WSEL latency with neuron growth is used for comparison among devices, which shows that the FPGA design outperforms CPU and GPU by 229 and 166 times respectively. The NTRAIN time for each sample depends on the size of the set ňb, which is a fraction of the number of neurons.

TABLE III: Hardware results and comparison

<table>
<thead>
<tr>
<th>Design Parameters</th>
<th>[23]</th>
<th>[24]</th>
<th>[22]</th>
<th>Proposed</th>
</tr>
</thead>
<tbody>
<tr>
<td>Feature Extractor</td>
<td>Inception-V3</td>
<td>Inception-V3</td>
<td>-</td>
<td>Resnet-18</td>
</tr>
<tr>
<td>Feat. Vec. dim</td>
<td>2048</td>
<td>2048</td>
<td>100</td>
<td>512</td>
</tr>
<tr>
<td>No. of Neurons</td>
<td>200</td>
<td>30</td>
<td>1000</td>
<td>2048</td>
</tr>
<tr>
<td>Output Classes</td>
<td>10</td>
<td>10</td>
<td>10</td>
<td>50</td>
</tr>
<tr>
<td>Network Params</td>
<td>409610</td>
<td>648050</td>
<td>1000000</td>
<td>1150076</td>
</tr>
<tr>
<td>Bit-Precision</td>
<td>16-bit</td>
<td>16-bit</td>
<td>16-bit</td>
<td>8-bit/16-bit</td>
</tr>
<tr>
<td>Mem. Requirement</td>
<td>1.3E+07</td>
<td>1.1E+07</td>
<td>1.6E+07</td>
<td>1.22E+07</td>
</tr>
</tbody>
</table>

Synthetic Results

Device: xc7vx690tffg | xcuv13p | xc7vx690t | xzcuv9eg
LUT: 265680 | 152546 | 232111 | 115656
FF: ~5000 | ~1000 | ~18400 | ~11840
DSP: 2048 | 2064 | 2064 | 1184
BRAM: (36kB) | 455 | - | 415.5 |
Max Frequency (MHz): | 209 | 204 | 93 | 200 |

VI. CONCLUSION

Lifelong learning on the edge is essential for autonomous agents operating in dynamic environments that need constant model adaptation. We proposed a FPGA based SONN that dynamically evolves to adapt to non-stationary data streams. In order to maintain scalability and reduce runtime, an efficient scheduling method is employed to maximize resource reuse and parallelism. We show that the proposed hardware approximation strategies not only resulted in shorter training time and lesser memory storage, but also improves accuracy. The proposed FPGA architecture also significantly outperforms the CPU and GPU implementations due to the effective use of application-specific parallelism and on-chip BRAM.

VII. ACKNOWLEDGEMENT

This work was supported in part by the National Research Foundation Singapore under its Campus for Research Excellence and Technological Enterprise (CREATE) Programme with the Technical University of Munich at TUMCREATE.